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CMOS Current-Frequency Signal Processing Unit for Bioimplantable Sensors

Madeline Nicole Threatt
University of Tennessee - Knoxville, mthreatt@vols.utk.edu

To the Graduate Council:

I am submitting herewith a thesis written by Madeline Nicole Threatt entitled "CMOS Current-Frequency Signal Processing Unit for Bioimplantable Sensors." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Syed K. Islam, Major Professor

We have read this thesis and recommend its acceptance:

Benjamin J. Blalock, Nicole McFarlane

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

CMOS Current-Frequency Signal Processing Unit for Bioimplantable Sensors

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Madeline Nicole Threatt

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I dedicate this work to my parents, whose love and support has never wavered.

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Abstract

Over the past few decades, implantable monitoring of glucose, lactate acid, and pH monitoring has become a viable replacement for stationary monitoring. Implantable biosensing requires biosensors in conjunction with corresponding potentiostats and a signal processing unit to translate the data information to a more versatile, transmittable form. This thesis presents a current-mode signal processing unit (SPU) that merges the simplicity of a charging capacitor in feedback topology with the accuracy of a delta-sigma modulator to create a pulse train with a frequency proportional to the input current. The SPU was realized in a 0.18 μ[micro]m bulk CMOS process.

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Chapter 1

Introduction

1.1 Diabetes

Diabetes is a disease that affects many people. According to the National Diabetes Statistic Report published in June 2014, 29.1 million people in the United States are diabetic [1]. Diabetes is caused when the body is unable to produce a sufficient amount of insulin. Insufficient amounts of insulin cause less glucose to be absorbed in the blood and glucose levels to be higher than desirable. Diabetes characterizes a lifestyle that demands constant monitoring of diet, exercise, and blood glucose levels. In order to monitor blood glucose levels, a blood sample must be obtained and tested periodically throughout a patient's day.

1.1.1 Mobile Glucose Monitoring

Over the past few decades, mobile glucose monitoring has become a viable replacement to stationary monitoring. In 1987, the first personal glucose meter was introduced by Medisense Inc. At the turn of the century, Cygnus Inc. launched a wearable noninvasive watchlike glucose monitor [2]. Currently, the most common handheld glucose monitors require patients to prick his or her finger to obtain a blood sample, then the sample is tested using a handheld device. However,

technological advances allow research towards an new method of mobile monitoring: implantable biosensing. Implantable biosensing implies that a microchip is implanted under the skin of the patient which monitors a patient's vital signals and sends the data to an external device. This method is relatively non invasive compared to traditional handheld glucose monitors that require blood samples throughout the day. Implantable biosensing also presents the possibility of continuously monitoring.

1.1.2 Other Vitals to be Monitored

Implantable biosensing can be applied to other vitals such as lactate acid, oxygen and pH concentrations. Such monitoring functions can be incorporated into a single implantable system.

Oxygen Saturation

A pulse oximetry is typically used to measure a patients' oxygen saturation. Oxygen saturation values are especially of interest for emergency medicine, patients with respiratory or cardiac problems, and patients with sleep disorders. In addition, those who participate in high altitude activities would also benefit from oxygen saturation monitoring.

Lactate Acid Concentration

Typically, oxygen is used to break down carbohydrates to produce energy. However, when blood oxygen levels are low, lactate acid is produced in the muscle cells and red blood cells. Lactate acid concentration is of interest during the diagnosis of "hypoxia, lactic acidosis, some acute heart diseases and drug toxicity tests [3]." High lactate acid is also relevant to those who participate in strenuous exercise.

pH Concentration

Slight variation in blood pH can cause significant regulatory effects throughout the human body [4]. Acid-base disorders include: respiratory acidosis, metabolic acidosis, metabolic alkalosis, and respiratory alkalosis [5]. Therefore, pH monitoring is of importance to those diagnosed with an acid-base disorder.

1.2 Implantable Biosensing System

A single implantable device has been realized to monitor afore mentioned vitals, (glucose, oxygen, lactate acid, and pH concentrations). This device translates various chemical properties of a patients blood into an electrical signal that can be processed and communicated to varies parties. Figure 1.1 illustrates an implantable biosensing system.

This device allows the user to select the vital signal to be monitored. The request is received and then decoded by the Sensor Activation Circuit. Assuming the request is for the patient's glucose concentration, the Glucose Sensor is enabled while the remaining sensors are disabled. Then the potentiostat outputs an electrical current proportional to the glucose concentration. The current is then processed by the Signal Processor which creates a pulse train with a frequency proportional to the input current. This signal is then transmitted back to the patient's cellular device. Implantable biosensing requires small low powered devices for minimal invasiveness while maintaining high accuracy [6].

1.2.1 Electrochemical Sensors

There are various types of biomedical sensors, commonly categorized into four sectors: conductivity/capacitance, potentiometric, amperometric, and voltammetric sensors.

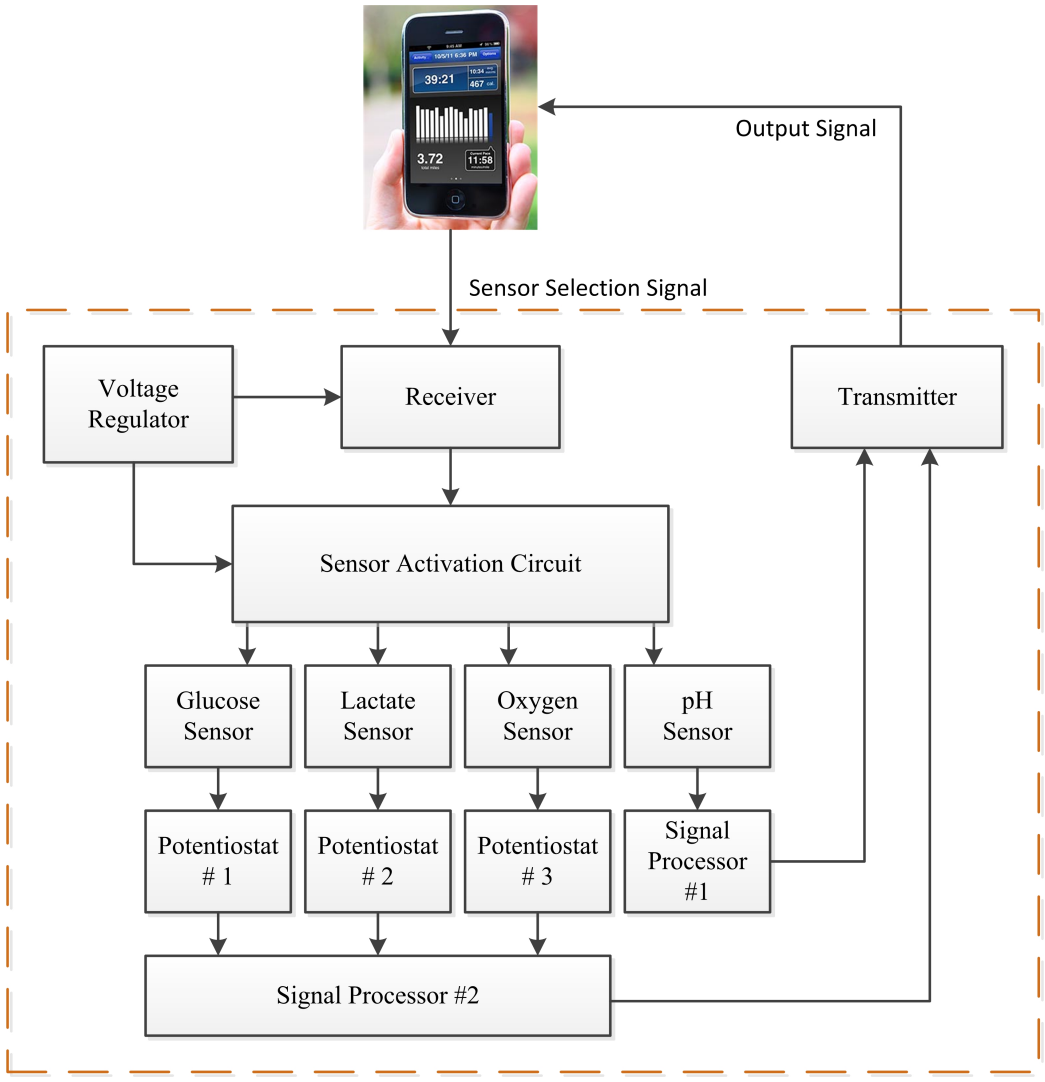

Figure 1.1: Block diagram of implantable biosensor system.

Conductivity/Capacitance Sensor

The conductivity/capacitance sensor measures the conductivity of a solution given the presence of the analyte under test. The conductivity of the solution, G (Ω^{-1}), is expressed in Equation 1.1 where A is the surface area of the electrode in (cm^2), and L is the distance between the electrodes (cm) [7]. The conductivity of the analyte, σ (Ω^{-1} cm^{-1}) is proportional to the concentration of the analyte.

$$G = \sigma \frac{A}{L} \tag{1.1}$$

However, the implementation of this method is complicated by Faradaic current (I_F), the current generated during the oxidation/reduction of the solution at the surface of the electrode, and the double layer formed adjacent to the surface of the electrode when a potential is applied on the sensor. These undesirable effects cause an inaccurate correlation between the conductivity of the solution and the concentration of the analyte and ultimately the conductivity/capacitance sensor to not be attractive for this biosensing application.

Potentiometric Sensor

Potentiometric sensors are based on the potential created at the surface of the electrode during the oxidation-reduction reaction. The created potential can be equated to the concentration of the analyte involved in the reaction, as shown in the Nernst equation (Equation 1.2) where E and E^0 are the electrode potential and the electrode potential at a standard state respectively, and a_{ox} and a_{red} are the activities of the oxidation reaction and the reduction reaction, respectively. Also, R is the universal gas constant, T is the temperature, Z is the number of electrons transferred, and F is Faraday's constant.

$$E = E^0 + \frac{RT}{ZF} ln \left(\frac{a_{ox}}{a_{red}} \right) f \tag{1.2}$$

For the potentiometric sensor to yield an accurate correlation, the sensor must operate in a thermodynamic equilibrium, implying that there is zero-current. However, reaching the equilibrium conditions required for the potentiometric sensor can take a long response time [7].

Voltammetric and Amperometric Sensors

The voltammetric and amperometric sensors are based on the current-potential relationship of the electrochemical cell. For an amperometric sensor, a fixed potential, E_i, is applied between the two electrodes causing a reduction or oxidation reaction to occur, and the resulting current, I_F, is measured. When the mass transfer condition is total diffusion, I_F linearly corresponds to the concentration of the analyte by Fick's law of diffusion as shown in Equation 1.3, where km is the mass transfer coefficient and C^* is the concentration of the analyte [7].

$$I_F = ZFkmC^* \tag{1.3}$$

In order for amperometric sensors to be effective, it is vital that E_i be fixed. Voltammetric and amperometric sensors are widely used because of their effectiveness and well established fundamentals and will be selected for this biosensing application.

Reference Electrodes

The potentiometric, voltammetric, and amperometric sensors require a reference electrode. For the potentiometric and amperometric sensors, the reference electrode serves as a counter and completes the circuitry. However, in modern amperometric sensors the mentioned reference electrode is divided between a counter electrode (CE) and a reference electrode (RE). The primary reaction occurs on the working electrode (WE). The RE is adjusted such that E_i remains constant across the WE and the RE. In addition, the RE draws no current. In contrast, the CE generates the "opposite current occurring that the surface of the WE in order to keep the charges neutral." [8] Figure 1.2 details the equivalent circuit model of a three electrode electrochemical cell. R_{WE}, R_{RE}, and R_{CE} are the Faradic resistances related to each of the electrodes. R_{S1} and R_{S2} are the analyte resistances. C_{CE} and C_{WE} are the electrode double-layer capacitances and are proportional to the surface area of each electrode.

$$R_{WE} = \frac{E_i}{I_F} \tag{1.4}$$

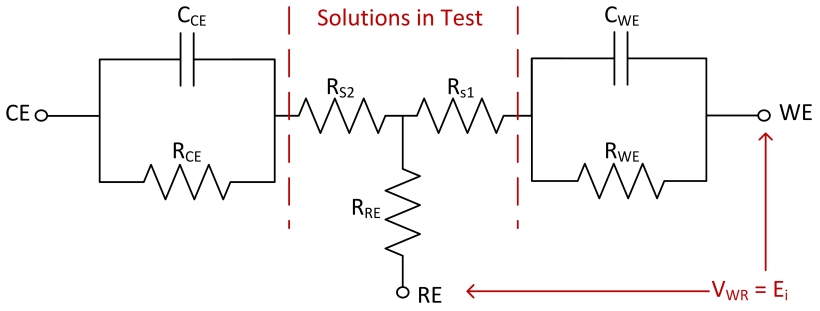

Figure 1.2: Equivalent circuit model of three electrode electrochemical cell.

1.2.2 Potentiostat for Voltammetric /Amperometric Sensors

Therefore, with the selection of an amperometric sensor for this implantable biosensing application, a potentiostat is required to ensure that the potential E_i is held constant. In addition, the potentiostat must be capable of accurately transferring the Faradaic current from the sensor to the SPU in order to maintain the linear correlation between the analyte concentration and the Faradaic current. There are two general categories of potentiostats: grounded WE and RE and grounded CE.

1.3 Overview of Thesis

In Chapter 1, an implantable biosensing system was introduced. In Chapter 2, various signal processing unit topologies will be discussed. Then the selected design will be explored in Chapter 3, and the simulated and experimental results will be presented in Chapter 4. Chapter 5 will present design changes for the next generation SPU. Lastly, conclusions and future work will be presented in Chapter 6.

Chapter 2

Literature Review

In order for implantable biosensing to be an effective alternative to stationary vital monitoring, the signal processor shown in Figure 1.1 must have a linear current-frequency relationship while operating with minimal power consumption and consuming little area. Signal processing units can be categorized into two main groups: charging capacitor in feedback and delta-sigma modulator. Section 2.1 describes capacitor in feedback systems and then discusses several examples; similarly, Section 2.2 explores delta-sigma modulators. These two schemes are then compared in Section 2.3, and finally, a hybid configuration will be discussed in Section 2.4.

2.1 Charging Capacitor in Feedback

Perhaps the simplest of current-frequency converters, a capacitor-based scheme allows the input current to accumulate charge over a capacitor. Once a voltage higher than that of a given reference has accumulated over the capacitor, the capacitor is then discharged. The switch from charging to discharging is preformed using feedback. The periodic switching creates a pulse train with a frequency proportional to the input current. The charging capacitor in feedback is attractive for bioimplantable sensing applications because of its simplicity and direct relationship between input

current and resulting frequency. References [9] and [10] report implementations of the charging capacitor approach.

Reference [9] proposes the current-frequency converter shown in Figure 2.1. The current, I_{conv}, is the current to be converted to a digital pulse train. When the voltage across the capacitor, C_p, has exceeded the voltage level, V_{up}, V_{out} is pushed high, opening the PMOS switch and allowing the capacitor to discharge by I_{conv}.The S-R latch ensures that the capacitor must be fully charged before the switch closes and discharging begins. Assuming a constant I_{conv}, the PMOS switch will be periodic and effectively a pulse train.

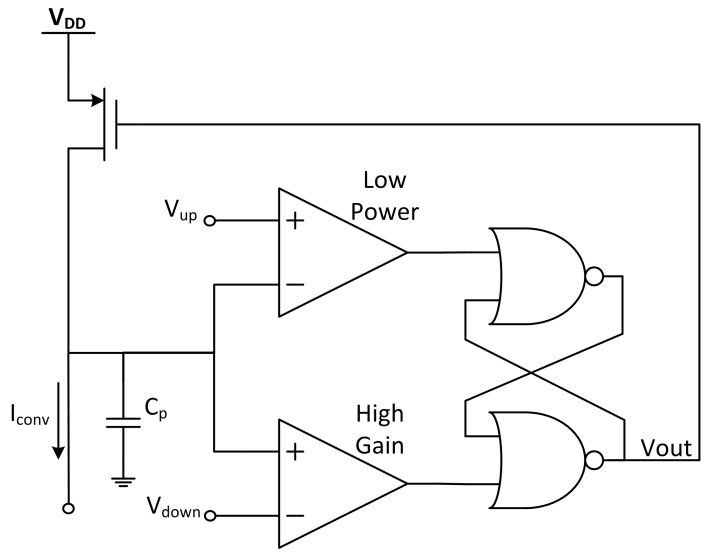

Figure 2.1: Schematic of SPU [9].

Reference [10] proposes the current-frequency converter shown in Figure 2.2. Assuming that the capacitor, C, is completely charged and the PMOS switch is open, the counter electrode current, I_{CE}, is used to discharge the capacitor. Once the capacitor is discharged below a low threshold set, the Schmitt Trigger outputs a logic '1', closing the PMOS switch. This recharges the capacitor and exceeds the upper threshold set by the Schmitt Trigger, causing the switch to open again. This

creates a pulse train with a characteristic frequency proportional to the discharge current.

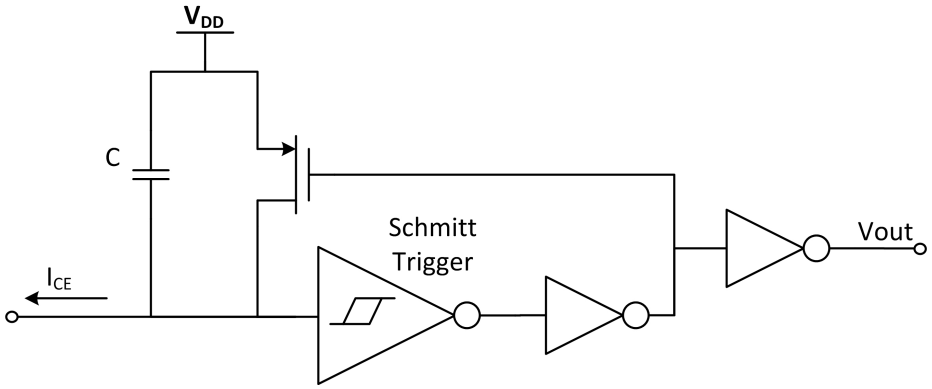

Figure 2.2: Schematic of SPU [10].

2.2 Delta-sigma Modulator

The second SPU topology is the delta-sigma modulator. Figure 2.3 depicts the block diagram of a first-order delta-sigma modulator.

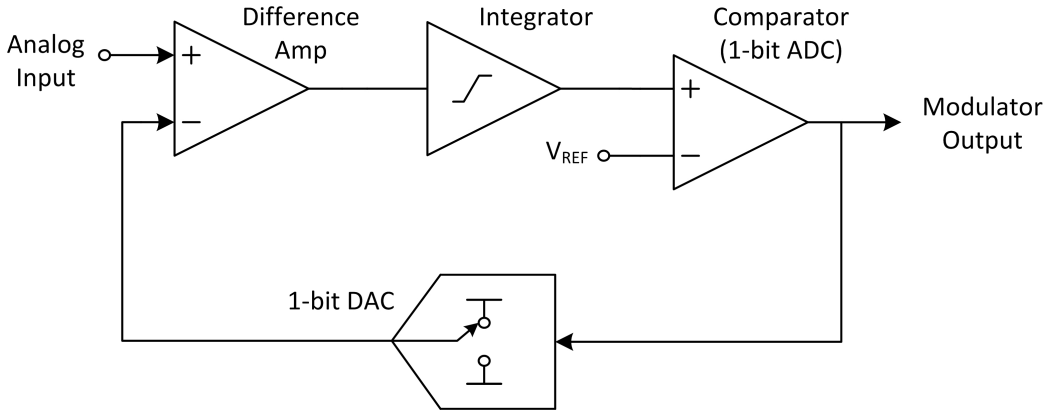

Figure 2.3: Block diagram of a first-order delta-sigma modulator.

Delta-sigma modulators consist of two elements, oversampling and noise shaping. Oversampling implies that the input signal is sampled at a frequency greater than the Nyquist rate, $f_S = 2B$ [11]. Oversampling occurs at the system's input using

the difference amplifier and the 1-bit digital-analog converter (DAC). The integrator effectively distributes the quantization noise across a larger spectrum than if sampled at the Nyquist rate. Therefore, Delta-sigma structures are characterized by high accuracy and low power consumption [12].

Delta-Sigma modulators produce a pulse-width modulated (PWM) output. Figure 2.4 details the PWM signal resulting from a simple sinusoidal input.

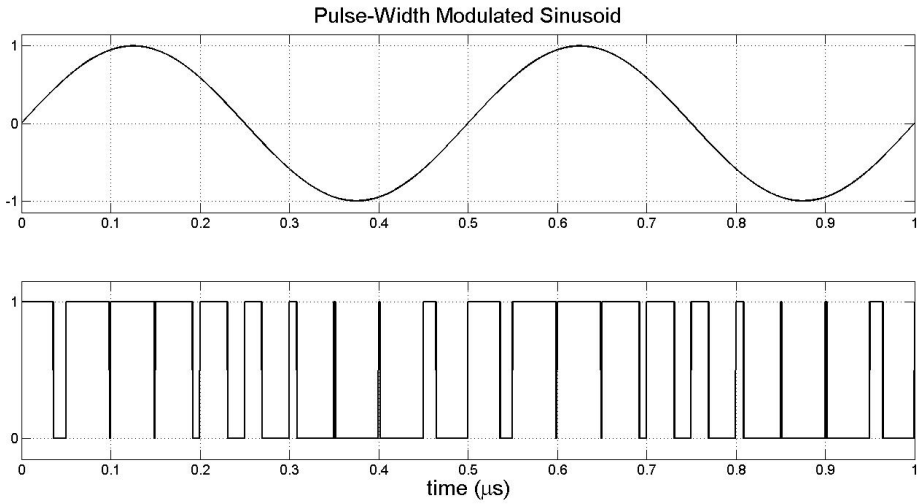

Figure 2.4: Pulse-width modulated sinusoid.

From Figure 2.4 it can be extrapolated that for a given point on the sinusoid, there is a corresponding pulse width. Therefore, if the input is constant, then the PWM output would be a pulse train with a consistent and hence characteristic frequency.

2.3 Comparison

Two SPU structures were discussed above, charging capacitor in feedback and the delta-sigma modulator. The charging capacitor in feedback is a simpler approach, while delta-sigma structures yield higher accuracy. Delta-sigma structures are also characterized by high frequency outputs, which is undesirable in implantable biosensing applications. However, high frequency outputs can be remedied through

the use of a demodulator, such as a low-pass filter or counter. Both schemes pose advantages and disadvantages for the biosensing application. Table 2.1 compares examples of charging capacitor in feedback and delta-sigma modulators.

Table 2.1: Work Comparison

	V_{DD}	Current Range	Frequency Range	Area	R^2 Value	Power Consumption
[9]	1.5 V	350 pA - 600 nA	370 Hz - 590 Hz	–	–	12μW
[10]	–	0.1 μA - 1.5 μA	–	2.5mm^2	0.9968	18μW

2.4 Capacitor in Feedback, Delta-Sigma Modulator Hybrid

In order to utilize the advantages presented by the charging capacitor in feedback and delta-sigma modulators, a third scheme has been realized that contains the simplicity of a capacitor in feedback with the accuracy of a delta-sigma modulator [13]. This scheme was selected for the SPU and will be explored in Chapter 3.

Chapter 3

Design

As discussed in Chapter 2, current-frequency SPUs can be categorized into two general groups: charging capacitor in feedback and delta-sigma modulator. Chapter 3 details the proposed structure for the 1.4 V current-frequency converter, which combines the simplicity of the charging capacitor in feedback with the accuracy of the delta-sigma modulator. This hybridization is achieved by replacing the integrator in Figure 2.3 with a charging capacitor circuit. Therefore, this system can also be considered a synchronous capacitor in feedback or simplified delta-sigma modulator.

Section 3.1 will discuss the functionality of the proposed SPU. Then Section 3.2 will present the input network of the system. Sections 3.3 and 3.4 will detail the functionality of the comparator and D flip-flop, respectively. Currents and capacitor sizing is detailed in Sections 3.6 and 3.5, respectively. A modulation scheme is discussed in Section 3.7. Finally, power improvements are presented in Section 3.8.

3.1 SPU Overview

The proposed structure is shown in Figure 3.1, where I_S is the sensor current, and I_B is a bias current.

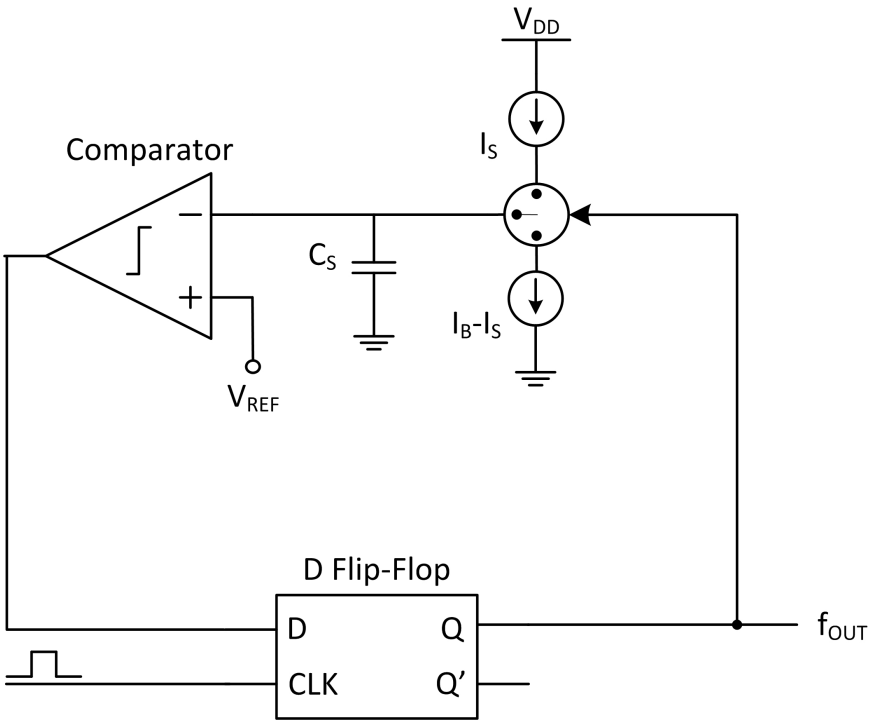

Figure 3.1: Simplified schematic of proposed SPU.

The switch in Figure 3.1 can effectively be represented as a switched current mirror as shown in Figure 3.2. This reduces the parasitic effects generated by connecting and disconnecting the sink current.

Similar to the charging capacitor in feedback, the source current, I_S, charges C_S. The voltage across a capacitor can be calculated using Equation 3.1; therefore, the charging voltage across the capacitor for time period, T_{charge}, can be summarized by Equation 3.2. T_{charge} can be expressed as an integer multiple of the clock period, T_{CLK}, such that $T_{charge} = n\ T_{CLK}$.

$$V(t) = \frac{1}{C}\int_{t_0}^{t} I(\tau)d\tau + V(t_0) \tag{3.1}$$

$$V_{charge} = \frac{I_S T_{charge}}{C_S} = \frac{I_S n T_{CLK}}{C_S} \tag{3.2}$$

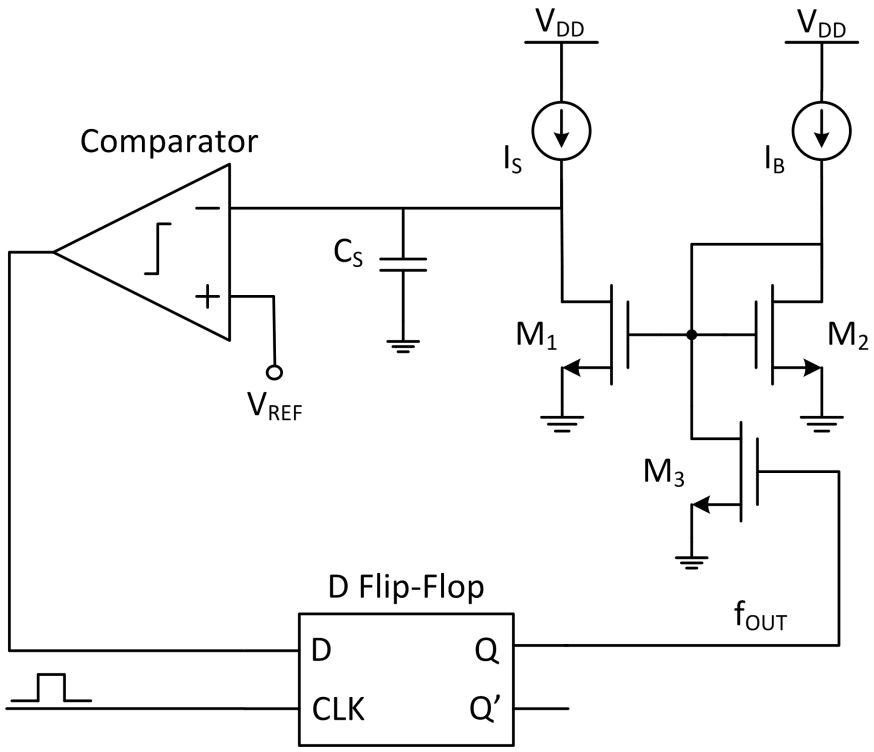

Figure 3.2: Schematic of proposed SPU.

The comparator outputs a logic '1' as long as the voltage across the capacitor is less than V_{REF}. This signal is then synchronized using the D flip-flop. The output is applied to the gate of M_3, turning the transistor *ON*. Therefore, the gates of M_1 and M_2 are grounded, and the source current continues to charge the capacitor. This continues as long as the voltage across C_S is less than V_{REF}, per Table 3.1. Figure 3.3 details this mode of operation.

Once voltage across C_S exceeds V_{REF}, the comparator outputs a logic '0' which is synchronized by the DFF. The output grounds the gate of M_3, turning the transistor *OFF*. The current mirror established between M_1 and M_2 requires that a matched current of I_B be pulled through M_1. Therefore, a current of $I_B - I_S$ is drawn out of C_S to compensate. Consequently C_S is discharged through M_1. This continues as long as the voltage across C_S is greater than V_{REF}. The discharging voltage across the capacitor for time period $T_{discharge}$ can be summarized by Equation 3.3, where

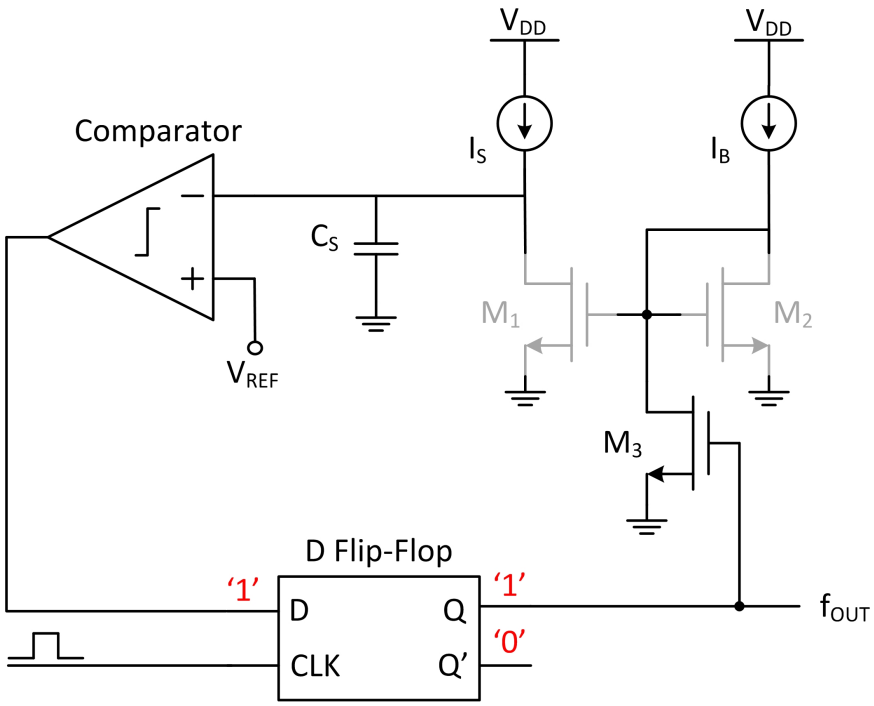

Figure 3.3: Schematic of proposed SPU in charge state.

$T_{discharge}$ can be expressed as an integer multiple of the clock period, T_{CLK}, such that $T_{charge} = m\ T_{CLK}$. Figure 3.4 details this mode of operation.

$$V_{discharge} = \frac{(I_B - I_S)T_{discharge}}{C_S} = \frac{(I_B - I_S)mT_{CLK}}{C_S} \tag{3.3}$$

It is can be assumed that the potential created across the capacitor during charging is equal to the potential removed from across the capacitor during discharging, allowing $V_{charge} = V_{discharge}$. Therefore, I_S and I_B can be related as in Equation 3.4, where n and m are integers representing the number of clock cycles required to charge and discharge C_S, respectively.

$$I_S(n+m) = I_B m \tag{3.4}$$

$$n = m\left(\frac{I_B}{I_S} - 1\right) \tag{3.5}$$

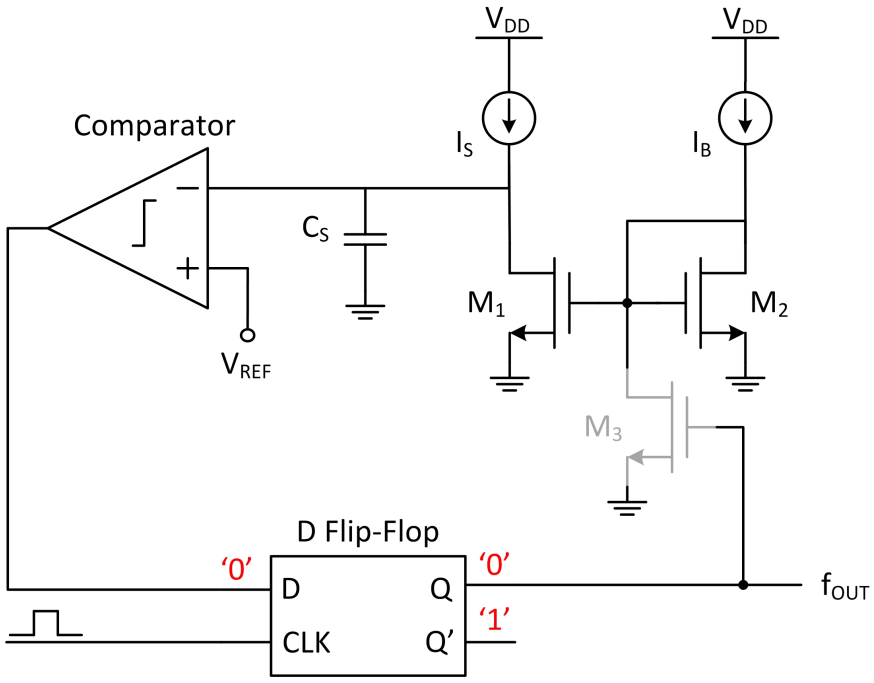

Figure 3.4: Schematic of proposed SPU in discharge state.

The time required to charge and discharge the capacitor can be considered the period of a single event; therefore, the period of an event is simply the time required to charge plus the time require to discharge the capacitor as shown in Equation 3.6. Notice that this function is independent of capacitance.

$$T_{event} = T_{CLK}(n+m) = \frac{mT_{CLK}I_B}{I_S} \tag{3.6}$$

Assuming that the capacitor is discharged within a single clock cycle, m can be set to 1. Therefore, the frequency of a charging even can be given by Equation 3.7.

$$f_{event} = \frac{I_S}{mT_{CLK}I_B} = \frac{I_S}{T_{CLK}I_B} \tag{3.7}$$

From Equation 3.7, it can be concluded that the output frequency of the proposed system is linearly correlated to the input current, I_S.

3.2 Input Network

Current mirrors were implemented instead of sourcing I_S and I_B directly to M_1 and M_2. This protects the switching circuit from current dividing caused by a matched current source impedance. Also, this scheme is a better representation of the complete system once the potentiostat is connected. The SPU input network is shown in Figure 3.5

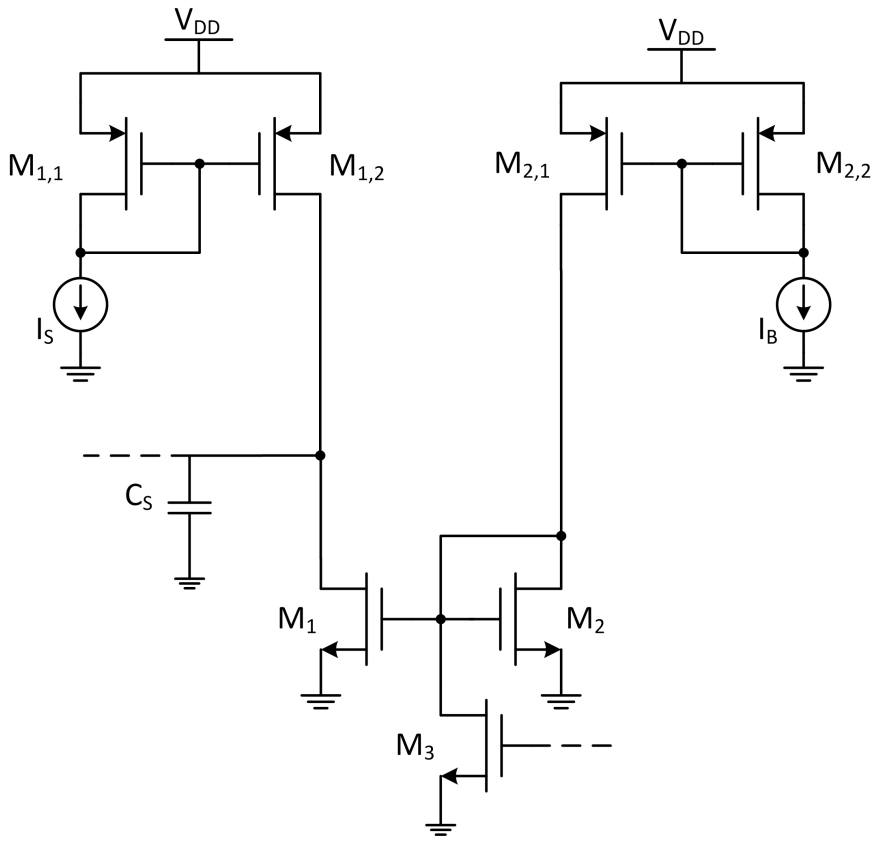

Figure 3.5: Schematic of proposed SPU input network.

3.3 Comparator

A cross-coupled PMOS comparator was implemented to compare the voltage across C_S to the reference voltage, V_{REF}. Figure 3.6 shows the topology of the comparator.

M_7 and M_8 create a current mirror that requires the combination of i_{IN} and i_{REF} to equal i_{bias}. M_3 - M_6 are considered to be the decision circuit and control the functionality of the comparator. Assuming V_{IN} is less than V_{REF}, then $V_{GS,IN}$ is less than $V_{GS,REF}$. This causes more current to be pulled through M_2 than M_1. Therefore, M_3 and M_6 are *ON*, and M_4 and M_5 are *OFF*. As i_{IN} increases and $V_{DS,M3}$ equals $V_{THN,M4}$, current through M_4 must increase, effectively decreasing the current through M_6. Therefore, $V_{Ds,M6}$ decreases and starts to turn *OFF* M_3.

In preparation for subsequent components, the comparator is followed by a series of inverters to buffer the output signal and allow rail to rail voltage swing. This insures that the DFF will appropriately differentiate a logic '0' from a logic '1' [14].

The functionality of the comparator can be summarized by Table 3.1.

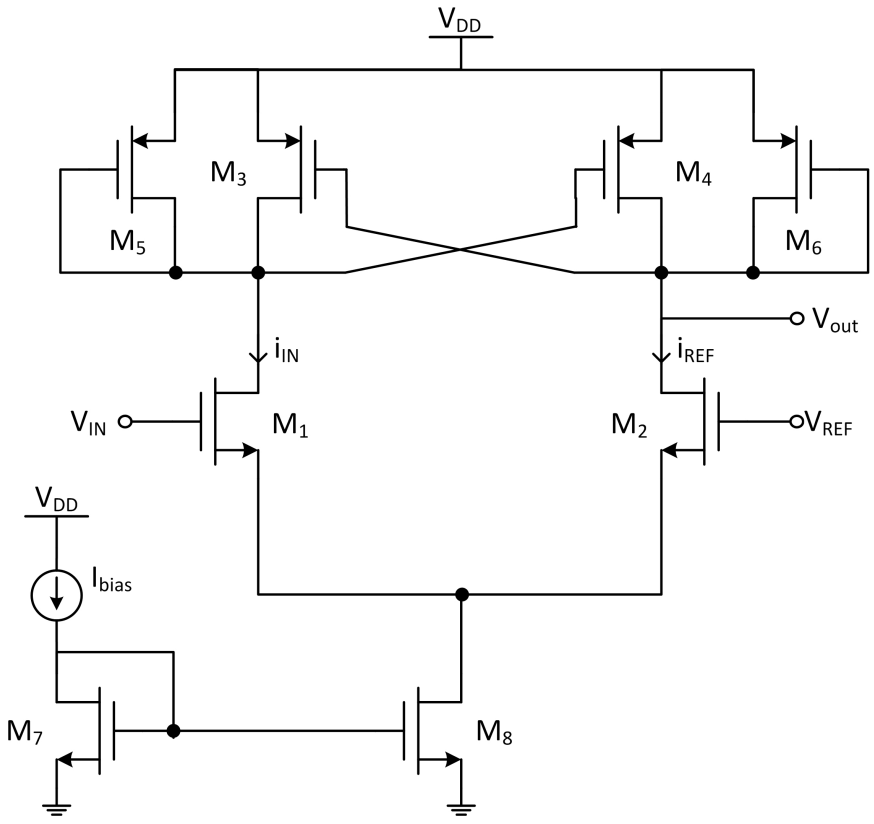

Figure 3.6: Schematic of designed comparator.

Table 3.1: Truth Table of Designed Comparator

V_{IN}	V_{OUT}
$< V_{REF}$	'1'
$> V_{REF}$	'0'

3.4 D Flip-Flop

D Flip-Flops (DFF) are one of the fundamental components within digital systems. DFFs synchronize an asynchronous input to a designated clock. The functionality can be summarized by Table 3.2. A standard master-slave topology was used to implement the DFF. The schematic can be shown in Figure 3.7.

Table 3.2: Truth Table of D Flip Flop

D	CLK	Q	$\overline{Q}$
0	0	previous state	
0	1	0	1
1	0	previous state	
1	1	1	0

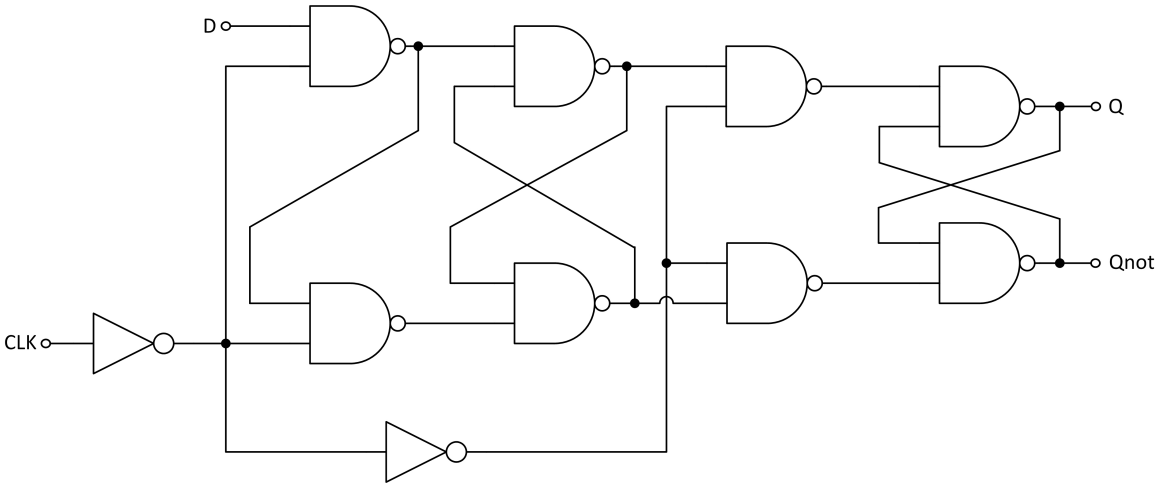

Figure 3.7: Schematic of designed master-slave DFF.

3.5 Capacitor C_S

The desired capacitance, C_S, can be calculated given Equation 3.2 and 3.3. With V_{REF} set to 700 mV, the change in V_{charge} is desired to be at least 700 mV in order to start the charging/discharging cycle, assuming zero initial charge stored in the capacitor. Since $V_{charge} = V_{discharge}$, Equation 3.8 steps through the calculation for the necessary C_S value.

$$\begin{aligned} V_{charge} = V_{discharge} &= \frac{(I_S - I_B)T_{charge}}{C_S} \\ 700mV &= \frac{(400nA - 100nA)}{C_S(500kHz)} \\ \therefore C_S &= 10pF \end{aligned} \tag{3.8}$$

As implied in Equation 3.10, the output frequency is independent of the capacitance value C_S. To verify, various values of C_S were simulated with I_S set to 100 nA, I_B to 400 nA, and f_{CLK} at 500 kHz; the resulting output frequencies were then compared, as shown in Figure 3.8. The average output frequency was 9.18 kHz with a standard deviation of 0.0165.

3.6 I_S and I_B

A problem arises when the values of I_S and I_B become close enough that over various charging cycles, the charging voltage is not constant; similarly, over various discharging cycles, the discharging voltage is not constant. This irregularity is shown in Figure 3.9, where $I_S = 300$ nA and $I_B = 400$ nA. In order to ensure that the charge and discharge voltage are equal, I_B is selected to be at least 4 times greater than I_S, causing $I_B - I_S$ to be 3 times greater than I_S.

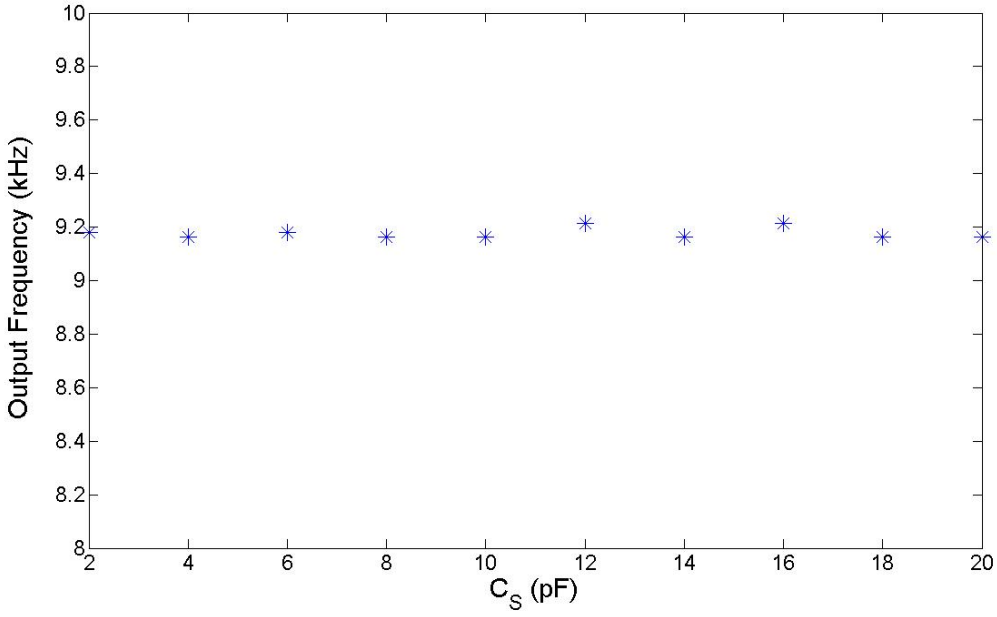

Figure 3.8: Output frequency for various values of C_S when $I_S = 100$ nA, $I_B = 400$ nA, and $f_{CLK} = 500$ kHz.

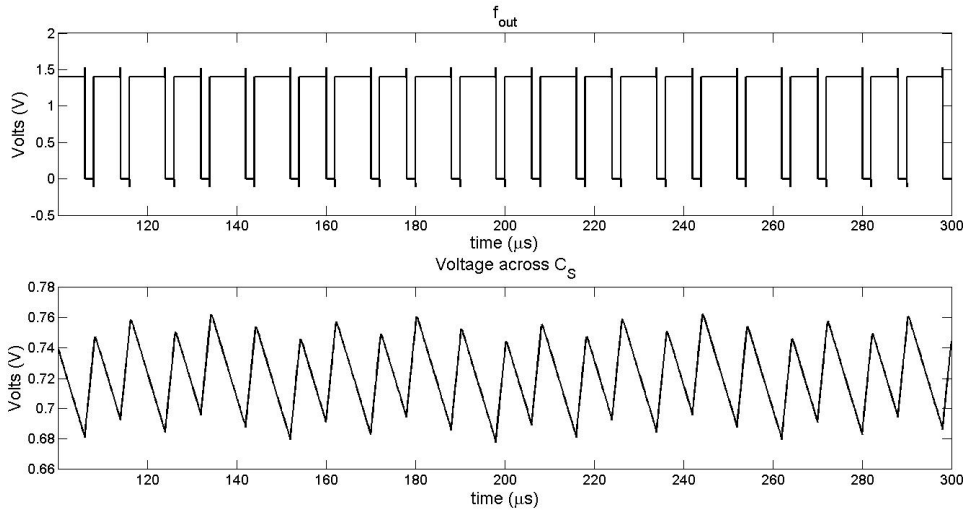

Figure 3.9: Irregularities amongst charging and discharging voltages caused by similar values of I_S and I_B.

3.7 Modulation Scheme

A counter can be used to modulate the f_{out} signal to a lower frequency. Equations 3.9 and 3.10 relate the period and frequency of the counter's b-bit to I_S, T_{CLK}, and I_B.

$$T_{MSB} = 2^b T_{event} = 2^b \frac{T_{CLK} I_B}{I_S} \tag{3.9}$$

$$f_{MSB} = \frac{1}{T_{MSB}} = \frac{I_S}{2^b T_{CLK} I_B} \tag{3.10}$$

In addition, by modulating the signal, any slight irregularities on the f_{out} signal will prove inconsequential to the final output, allowing the system to tolerate a larger range of I_S without sacrificing linearity. Therefore, increasing the number of bits of counter improves accuracy while also decreasing the MSB frequency. Figure 3.10 illustrates the described error tolerance for a 4-bit counter. Notice that both Ideal f_{out} and Errors in f_{out} correspond with the 4-bit Counter Output. Therefore, only those irregularities which fall on the rising edge of the nth-bit or the falling edge of the 2*nth-bit will be translated to the output.

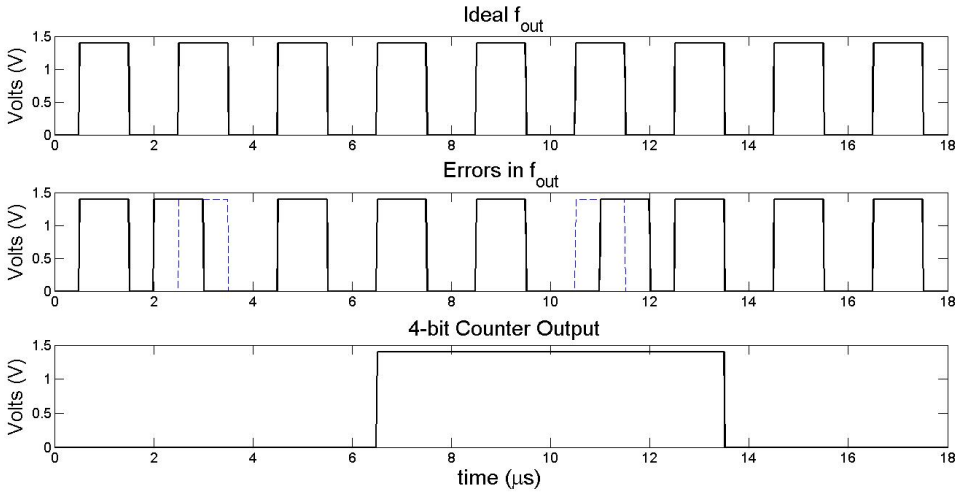

Figure 3.10: Example of increased accuracy by utilizing 4-bit counter.

3.8 Power improvement by varying I_S and T_{CLK}

According to Equation 3.10, I_S and T_{CLK} can be decreased, while maintaining the ratio of I_S to T_{CLK} in order to maintain linearity. For example, assuming I_S = 10 nA, I_B = 400 nA, and f_{CLK} = 500 kHz, the resulting f_{MSB} = 781 Hz from a 4-bit counter. Likewise, for the same source current, f_{MSB} = 781 Hz when I_B = 40 nA and f_{CLK} = 50 kHz.

$$f_{MSB} = \frac{I_S f_{CLK}}{2^b I_B} = \frac{10nA(500kHz)}{2^4(400nA)} = \frac{10nA(50kHz)}{2^4(40nA)}$$

Figure 3.11 graphically represents the current-frequency relationship described by Equation 3.10 using an adjusted I_B and T_{CLK}.

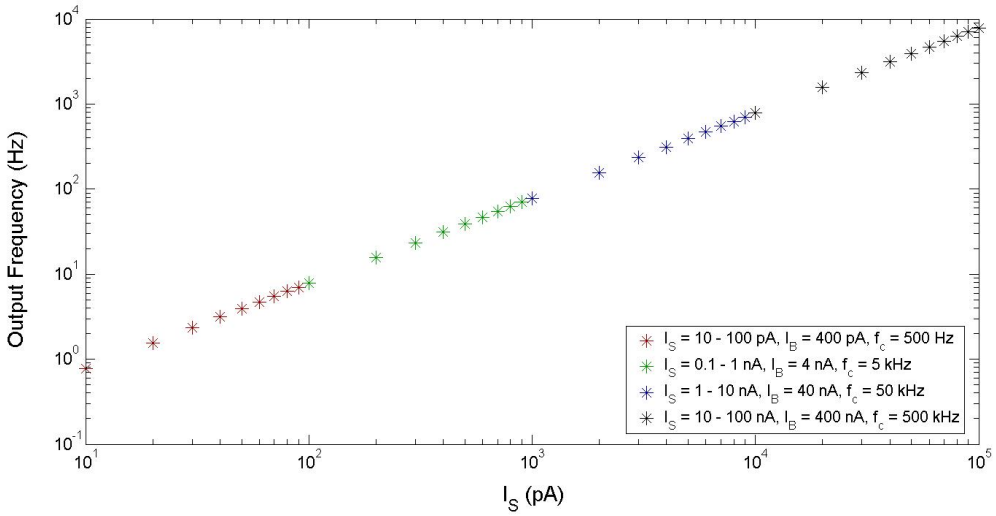

Figure 3.11: Plot of Equation 3.10 for various values of I_S.

By altering I_S and T_{CLK}, the power consumption significantly decreases.

Chapter 4

Simulated and Experimental Results

The proposed SPU has been designed and fabricated in a standard 0.18 μm bulk CMOS process with a 1.4 V power supply. Sections 4.1 and 4.2 detail the testing preformed on the comparator and DFF, respectively. Next the system performance will be discussed in Section 4.3. Finally, in Section 4.4 the power consumption of the system will be compared to other schemes.

The layout of the proposed SPU can be found in Figure 4.1. The system occupies 300 μm by 118 μm or 0.035 mm^2.

The chip microphotograph is shown in Figure 4.2. Unfortunately due to required metal fills, the circuit is indecipherable; therefore, the padframe layout is overlaid on top of the microphotograph in order to provide a size context. Two versions of the system were implemented and can be seen in the figure.

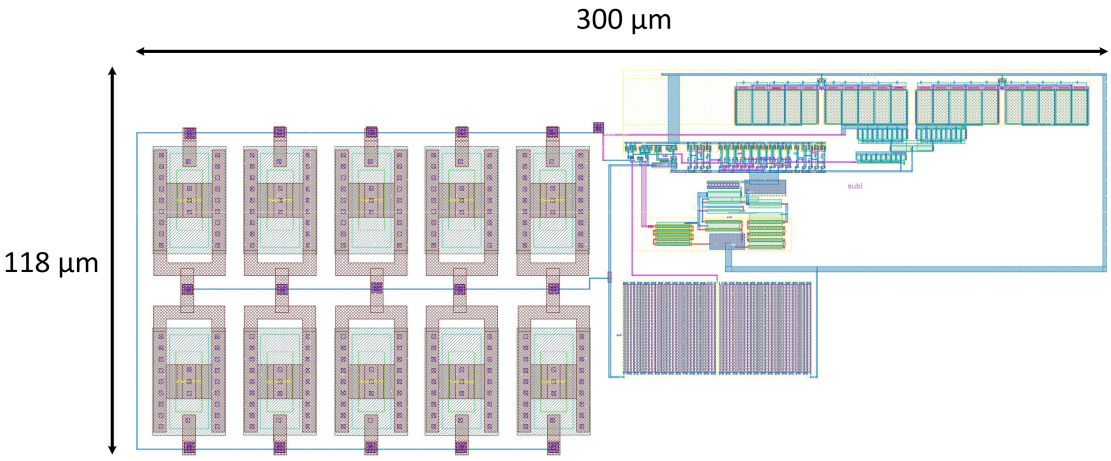

Figure 4.1: Layout of proposed SPU.

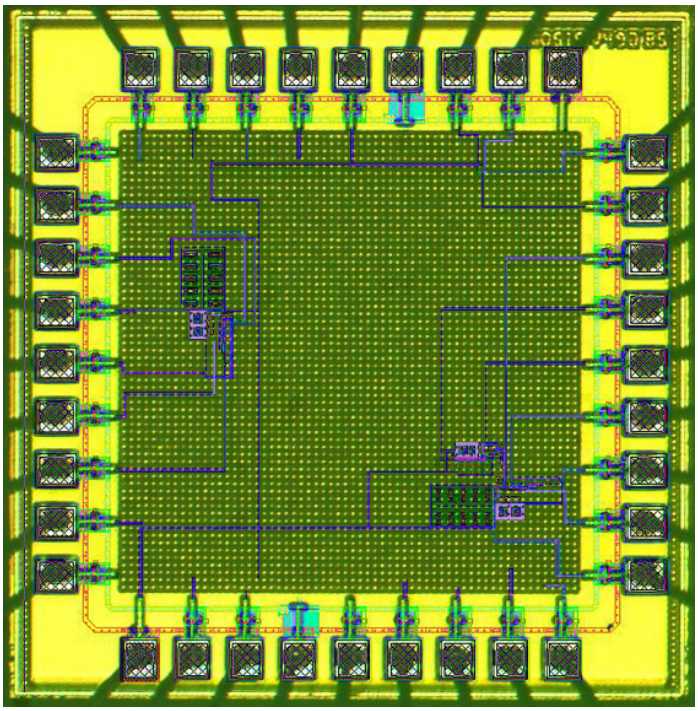

Figure 4.2: Microphotograph of SPU implemented in 0.18 μm bulk CMOS process with overlaid padframe layout image.

4.1 Comparator

The comparator was experimentally tested using an I_{bias} of 200 nA, V_{REF} of 0.7 V, and a 10 kHz, 1.4 V_{pp} triangular input is applied to mimic the accumulation of charge of the capacitor. The result is shown in Figure 4.3. The comparator functions as expected such that when $V_{IN} < V_{REF}$, the output is a logic '1' and when $V_{IN} > V_{REF}$, the output is a logic '0'.

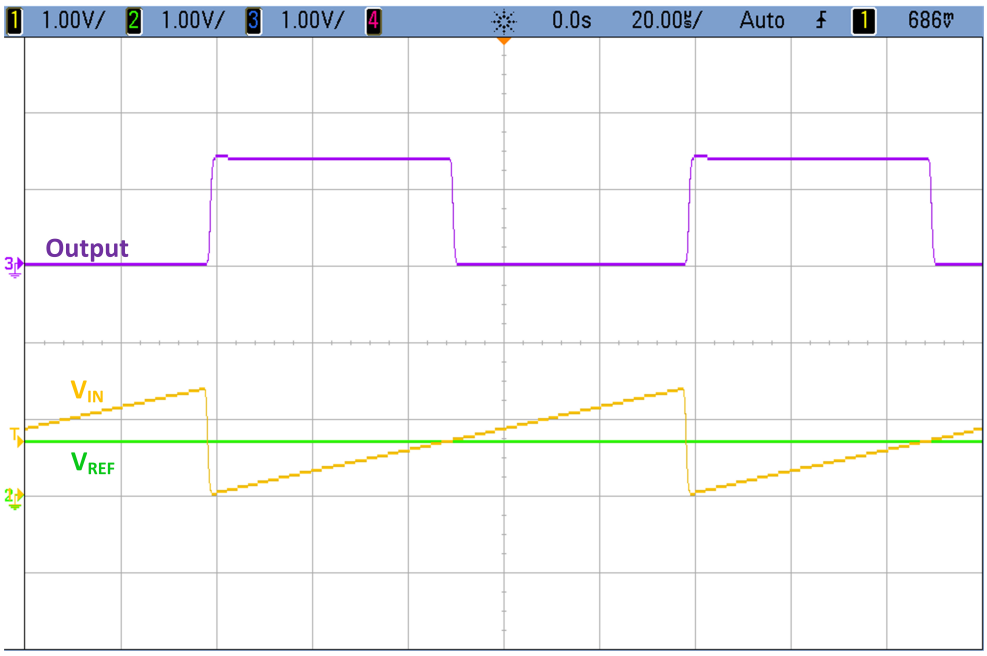

Figure 4.3: Comparator output when $I_{bias} = 200$ nA, $V_{REF} = 0.7$ V, and a 10 kHz, 1.4 V_{pp} triangular input is applied.

4.2 D Flip-Flop

The DFF was experimentally tested using a 500 kHz clock and 100 kHz 1.4 V_{pp} input. The result, as shown in Figure 4.4, accurately outputs the input signal on the rising edge of the clock. The jitters in the output can be attributed to clock feedthrough.

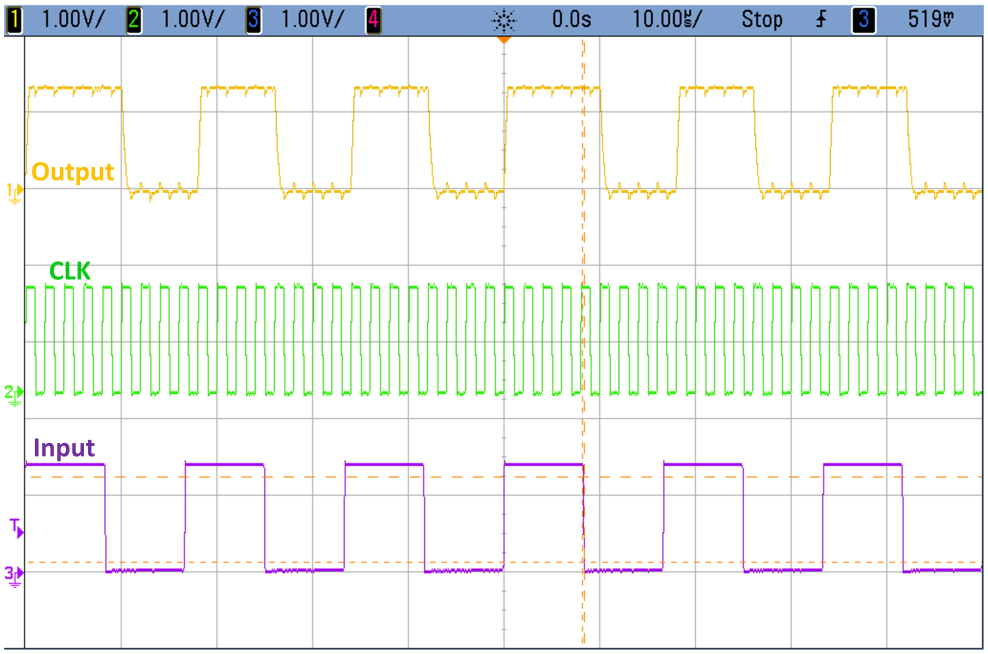

Figure 4.4: DFF Output when 100 kHz, 1.4 V_{pp} input is applied and f_{CLK} = 500 kHz.

4.3 Overall System

Prelayout simulation yielded a current-frequency relationship as shown in Figure 4.5, with a coefficient of determination, R^2, equal to 0.999992.

For experimental testing, I_S, I_B, and I_{bias} were sourced using a source meter, and the system clock was generated using a function generator. The premodulated system output when I_S = 100 nA, I_B = 400 nA, and f_{CLK} = 500 kHz can be found in Figure 4.6 to be 250 kHz. This result does not align with the anticipated performance of 147 kHz. Other current configurations were experimentally tested; for each, the output frequency was exactly half of the clock frequency. This behavior indicates that I_S and I_B are undesirably similar in value and are each charging and discharging the capacitor in a single clock cycle.

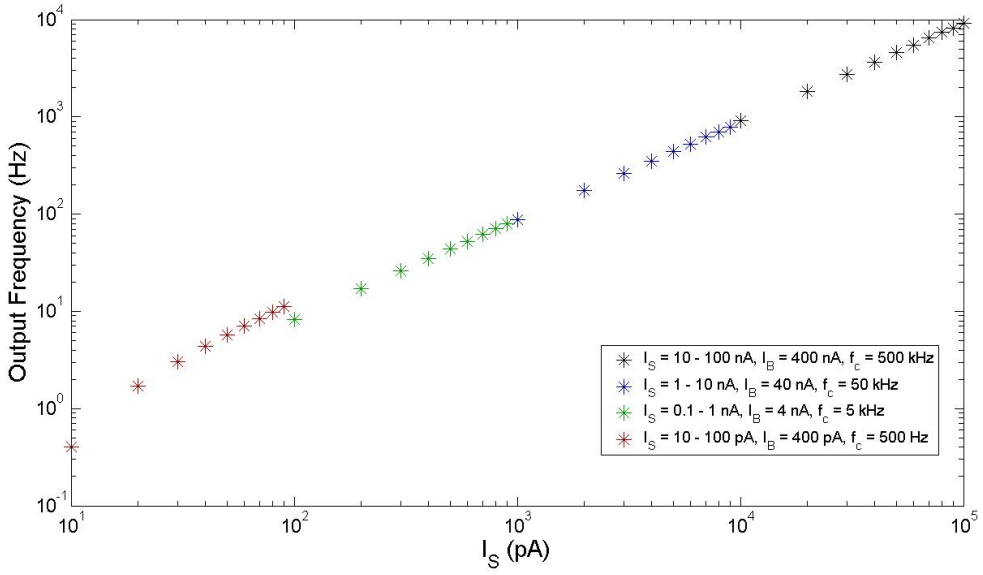

Figure 4.5: Simulated prelayout output frequency for various values of I_S.

4.4 Power Consumption

Table 4.1 compares the proposed scheme to those afore mentioned in Chapter 2.

Table 4.1: Presented SPU Compared to Previous Schemes

	Current Range	Frequency Range	Area	R^2 Value	Power Consumption
[9]	350 pA - 600 nA	370 Hz - 590 Hz	–	–	12μW
[10]	0.1 μA - 1.5 μA	–	2.5 mm^2	0.9968	18μW
Presented	10 pA - 100 nA	402 Hz - 9.17 kHz	0.035 mm^2	0.999992	5μW

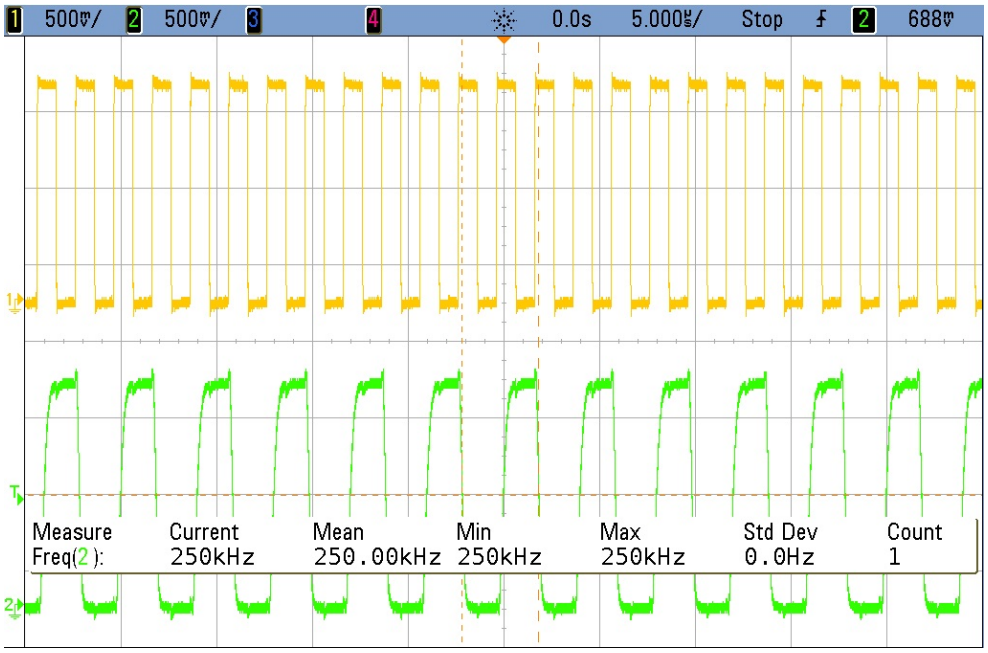

Figure 4.6: Experimental output frequency for I_S = 100 nA, I_B = 400 nA, and f_{CLK} = 500 kHz.

Chapter 5

Next Generation

Because the first generation SPU did not function as expected, several design improvements have been explored and will be discussed in this section.

5.1 ESD Protection

As presented in Section 4.3, experimental testing did not produce expected results. Instead, the output frequency was consistently half of the clock frequency. This implies that the system charges in a single clock cycle and then discharges in a single clock cycle. A possible cause could be ESD diode leakage current that is much greater than I_S and I_B causing the current through M_1 and M_2 to be undesirably similar in value. The simplest approach to eliminating this leakage current is to remove the ESD protection. Once fabricated, the chip would have to be handled carefully as to not damage the now unprotected device.

5.2 Low-voltage MOS Cascode Bias Circuit for I_{in} and I_B

A Minch Cascode Bias Circuit was implemented for both the source and bias current in order to improve the accuracy of the system. A schematic of this circuit is shown in Figure 5.1 [15] [16].

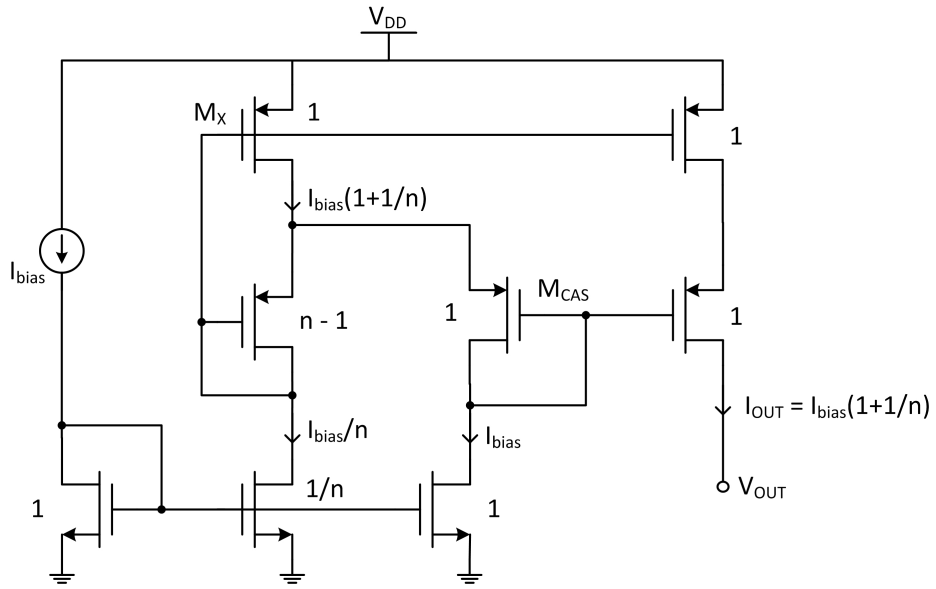

Figure 5.1: Schematic of Minch low-voltage MOS cascode bias circuit.

Equation 5.1 expresses the ratio of the forward current to the reverse current through transistor M_X as an integer, n. When the forward current is much larger than the reverse current, M_X is guaranteed to always operate in saturation.

$$n^2 = \frac{I_{F,MX}}{I_{R,MX}} \tag{5.1}$$

This value is then used to size the transistors. The Minch circuit is powerful, because the top device of the low-voltage cascode current mirror (the top right device) is biased such that it operates at the edge of saturation, maximizing the output compliance and increasing the wide dynamic range to be more than that of a simple

current mirror. Also, the larger the value of n, the more similar I_{OUT} becomes to I_{bias}. The value of n is dictated by the minimum and maximum device sizes allowed by the process. The increase in I_{OUT} from I_{bias} will only increase the output frequency while maintaining a linear relationship with I_{bias}. Therefore, the current amplification has little effect on the system's linearity.

M1 and M2 are then sized such that their leakage current is equal to that of the above PMOS cascode devices, effectively sinking the PMOS leakage current. This allows the small input current to not be overpowered by the leakage current. Figure 5.2 details the complete input system.

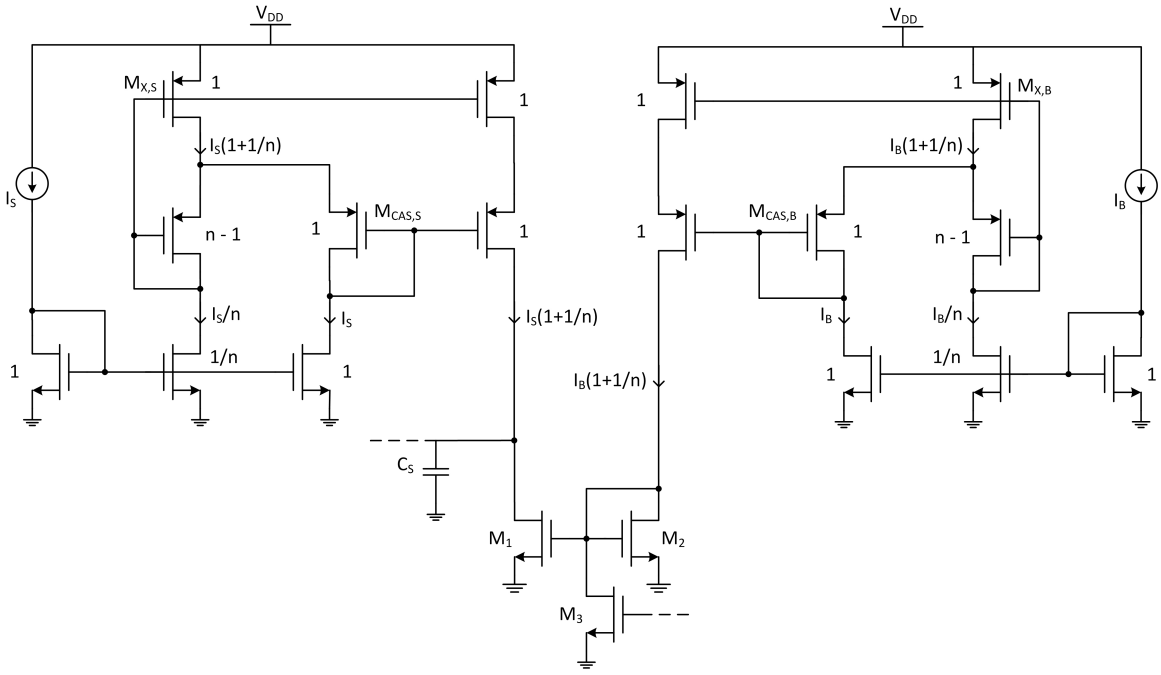

Figure 5.2: Schematic of Minch low-voltage MOS cascode bias circuit incorporated into proposed SPU input stage.

5.3 D Flip-Flop

In Section 4.2, the results from experimental testing show the presence of clock feedthrough in the output signal of the DFF. Therefore, for the second generation, a standard DFF will be implemented in hopes of eliminating this undesired effect.

5.4 Common Drain Voltage Buffer on C_S

The next generation of the SPU will include a common drain amplifier attached to the capacitor node. This would allow the accumulation of voltage of the capacitor to be monitored without affecting the monitored signal. The gain of the amplifier is described in Equation 5.2. With a desired gain of 1, the combination of $g_m R_s$ should be much larger than 1.

$$A_v = \frac{g_m R_s}{g_m R_s + 1} \tag{5.2}$$

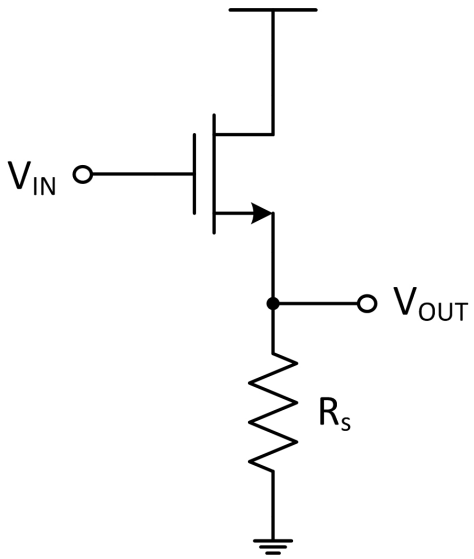

Figure 5.3: Schematic of simple common drain amplifier.

Chapter 6

Conclusion

Many diseases such as diabetes require patients to continuously monitor their vitals. Traditionally, a patient must obtain a blood sample by pricking his or her finger. However, technological advances present a new solution to this problem. Implantable biosensing has the potential to continuously monitor a patients vitals painlessly. As discussed in Chapter 1, this scheme requires a signal processor to convert a current containing the concentration information of the vitals into a pulse train where the frequency contains the desired information. The design of a current-frequency SPU has been presented in Chapter 3. The design was realized in a 0.18 μm bulk CMOS process, and the test results were discussed in Chapter 4. Chapter 5 then detailed improvements in the next generation of SPU.

6.1 Future Work

Future work includes automating the I_B and f_{CLK} selection according to the sensor current. This could be accomplished by establishing the range of I_S by comparing it to several bias currents; the output of the comparators could then close a switch allowing the appropriate I_B to bias the system. The comparators output could also be used to select the corresponding biasing for a tunable ring oscillator of a given frequency. However, this straight forward scheme could be improved to consume less

power, as all biasing current would continuously on for a continuous system. Per bioimplantable applications, decreasing the area and power consumption of the SPU while maintaining or improving the linearity is desired. Finally, the SPU should be tested using the selected potentiostat in order to guarantee system compatibility.

Bibliography

[1] Centers for Disease Control, Prevention, et al. National diabetes statistics report: estimates of diabetes and its burden in the united states, 2014. *Atlanta, GA: US Department of Health and Human Services*, 2014. 1

[2] Joseph Wang. Glucose biosensors: 40 years of advances and challenges. *Electroanalysis*, 13(12):983, 2001. 1

[3] You Wang, Hui Xu, Jianming Zhang, and Guang Li. Electrochemical sensors for clinic analysis. *Sensors*, 8(4):2043–2081, 2008. 2

[4] John A Kellum. Determinants of blood ph in health and disease. *Critical Care*, 4(1):6, 2000. 3

[5] Julian L Seifter. Acid-base disorders. *Cecil Textbook of Medicine, 22nd ed. Philadelphia, PA: WB Saunders*, pages 688–699, 2004. 3

[6] Santhisagar Vaddiraju, Ioannis Tomazos, Diane J. Burgess, Faquir C. Jain, and Fotios Papadimitrakopoulos. Emerging synergy between nanotechnology and implantable biosensors: A review. *Biosensors and Bioelectronics*, 25(7):1553 – 1565, 2010. 3

[7] Chung-Chiun Liu. *Electrochemical Sensors*. CRC Press, 2015/02/24 1999. 4, 5, 6

[8] Liang Zuo. Low-voltage bulk-driven amplifier design and its application in implantable biomedical sensors. *Doctoral Dissertations*, 2012. 6

[9] S. Carrara, M.D. Torre, A. Cavallini, D. De Venuto, and G. De Micheli. Multiplexing ph and temperature in a molecular biosensor. In *Biomedical Circuits and Systems Conference (BioCAS), 2010 IEEE*, pages 146–149, Nov 2010. ix, 9, 12, 29

[10] R.A. Croce, S. Vaddiraju, A. Legassey, S.K. Islam, F. Papadimitrakopoulos, and F.C. Jain. Low-power signal processing methodologies for implantable biosensing platforms. In *Signal Processing in Medicine and Biology Symposium (SPMB), 2013 IEEE*, pages 1–5, Dec 2013. ix, 9, 10, 12, 29

[11] Dallas Maxim. Demystifying sigma-delta adcs. *A/D and D/A Conversion/Sampling Circuits*, 2003. 10

[12] David Jarman. A brief introduction to sigma delta conversion. *Application Note AN9504, Intersil Corporation*, pages 1–7, 1995. 11

[13] Melika Roknsharifi. A low-power, highly stabilized three-electrode potentiostat using subthreshold techniques. *Doctoral Dissertations*, 2012. 12

[14] R Jacob Baker. *CMOS: circuit design, layout, and simulation*, volume 18. John Wiley & Sons, 2011. 19

[15] John D Cressler and H Alan Mantooth. *Extreme environment electronics*. CRC Press, 2012. 32

[16] Bradley A Minch. A low-voltage mos cascode bias circuit for all current levels. In *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, volume 3, pages 619–622. IEEE, 2002. 32

Vita

Madeline Threatt was born in Murry, KY, on 13 November 1992, the daughter of Timothy and Pamela Threatt. She and her family moved to Knoxville, TN in 1994. After graduating from Halls High School, she attended the University of Tennessee, Knoxville studying Electrical Engineering. Madeline completed an internship with Siemens Molecular Imaging from May 2012 to December 2012. In May of 2014, she completed her undergraduate career and graduated with the highest honors. A month later, she began her graduate studies at her undergraduate alma-mater under Professor Syed Kamrul Islam with a concentration in solid-state circuits.